CLAIM REJECTIONS UNDER 35 U.S.C. §§ 102 and 103

Independent claim 2 provides a method of forming a semiconductor device. The method includes, *inter alia*, providing a semiconductor substrate having first and second regions directly adjacent one another. Halogen-containing impurities are introduced into an exposed surface of the semiconductor substrate to form a higher halogen concentration in the first region than in the second region. Hence, as required by claim 2, the halogen-containing impurities are introduced directly into the exposed surface of the substrate, with the substrate having first and second regions directly adjacent one another.

In contrast to claim 2, Grider fails to disclose, teach or suggest such a method. First, Grider requires the introduction of halogen-containing impurities through a dummy gate oxide 34. Further, the two regions in Grider are clearly separated by isolation structure 32. Hence, the two regions are not directly adjacent one another. Finally, Grider appears to be using halogen-containing impurities to retard oxidation. Such a use teaches away from Applicants' invention which uses halogen impurities to enhance oxidation. For at least these reasons, independent claim 2 is allowable over Grider.

Claim 2 also is allowable over the prior cited reference Takagi. First, Takagi is directed to the formation of an isolation structure, as opposed to the creation of an oxide layer of varying thicknesses for the formation of active devices thereon. Secondly, as recognized by the Examiner, Takagi fails to address the use of halogen impurities. Hence for at least the above reasons, independent claim 2 is allowable over the prior cited art. Claims 4, 5 and 8-16 all depend from claim 2 and are allowable for at least depending from an allowable independent claim.

Independent claim 6 provides a method of forming a semiconductor device including, *inter alia*, introducing halogen-containing impurities into a first substrate region at a first concentration, and into a second region at a second concentration. Both the first and second concentrations are greater than 1×10^{14} carriers/cm^2. Such a method is clearly allowable over Grider. First, Grider fails to disclose the introduction of halogen-containing impurities at two different concentrations into two different regions. Grider is directed to the implantation of halogen species into only a single region, while protecting a second region from the halogen species (see Fig. 4). Further, claim 6 requires that the first and second

concentrations both be greater than 1 x10^{14} carriers/cm^2. Grider fails to disclose such a concentration level, and in fact teaches away from same by noting that the "doses [are] on the order of 1E12 to 1E14". Further, Grider teaches it is beneficial to use the low concentrations provided therein, and in fact has a preferred embodiment using fluorine or chlorine at a dose of about 5E12. (See Col. 3, lns. 35-41). As previously noted, claim 6 requires a much larger concentration of halogen-containing impurities. Hence for at least the above reasons, independent claim 6 is allowable over the cited art. Claim 7 depends from claim 6 and is similarly allowable.

Independent claim 20 provides a method of forming a semiconductor integrated circuit. The method includes selectively implanting halogen-containing impurities, having a concentration greater than 1 x 10^{14} carriers/cm^2, at an implant energy that is about 0.1 keV to about 40 keV. Hence for at least the reasons discussed in conjunction with claim 6, independent claim 20 is allowable over the cited art Grider. More specifically, Grider fails to disclose, teach or suggest the specific concentration of halogen-containing impurities that is required by claim 20. Further, claim 20 has the additional limitation of requiring that implant occur at a specific implant energy. Again, Grider fails to disclose, teach or suggest such a limitation. For at least these reasons, claim 20 is allowable over the cited art. Claim 21 as amended, and claims 22 and 23 all depend from claim 20 and are allowable for at least depending from an allowable independent claim. Further, dependent claim 21 clarifies the halogen concentration in the second region to be within a range that is clearly outside the range required by Grider.

Independent claim 24 provides a method of forming a semiconductor device. The method includes providing a semiconductor substrate having first and second regions directly adjacent one another. The method includes performing an oxidizing process on the semiconductor to simultaneously form first and second oxide layer thicknesses at first and second regions, respectively. The oxidizing process comprises a thermal anneal at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours. As previously noted, Grider fails to disclose, teach or suggest the formation of two regions having different oxide layer thicknesses in a single step whereby the two regions are adjacent one another. Further, Grider is silent as to the process for creating the oxide layer,

whereas claim 24 clearly sets forth a particular limitation with respect to the thermal anneal process. Hence, for at least these reasons, claim 24 is allowable over the cited art. Claims 25 and 26 depend from claim 24 and are allowable for at least depending from an allowable independent claim.

Independent claim 27 provides a method of forming a semiconductor device including, *inter alia*, introducing halogen-containing impurities into a first region and a second region whereby the concentration level of halogen impurities into the two regions are different from one another and both in excess of 1×10^{14} carriers/cm^2. For at least the reasons described in conjunction with prior claims, including claim 6, independent claim 27 is allowable over the cited art. Claim 28 depends from claim 27 and is similarly allowable.

Added claims 29-31 comprise three dependent claims directed to additional novel features of the present invention, some of which have been incorporated into the independent claims herein. Hence, claims 29-31 are allowable for at least depending from an allowable independent claim, and for the further novel features embodied therein.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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APPENDIX A

A clean copy of the claims is provided below in accordance with 37 CFR § 1.121(c). All pending claims are set forth below for convenient reference.

2. (Twice amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, said first region directly adjacent said second region;

introducing a halogen-containing impurities into an exposed surface of said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

forming a first memory gate electrode on said second oxide layer thickness, said second oxide layer thickness formed on said semiconductor substrate in a memory region.

4. (As previously amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises an ion implantation.

5. (As previously amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said first region and wherein said second region has substantially no halogen concentration therein.

6. (Twice amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said first region at a first concentration and introducing halogen-containing impurities into said second region at a second concentration, said first concentration greater than said second concentration, both said first and second concentrations having greater than 1×10^{14} carriers/cm^2.

7. (As previously amended) The method of claim 6 wherein introducing said halogen-containing impurities comprises an ion implantation.

8. (As previously amended) The method of claim 2 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

9. (As previously amended) The method of claim 2 wherein said semiconductor substrate also includes a third region where a third oxide layer thickness is desired, and wherein introducing said halogen-containing impurities also introduces halogen-containing impurities such that a different halogen concentration is formed in said third region than in said first region and in said second region.

10. (As previously amended) The method of claim 2 wherein said semiconductor device comprises a flash EEPROM semiconductor device.

11. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a floating gate electrode.

12. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a stack gate cell.

13. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a split gate cell.

14. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a control gate electrode.

15. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a stack gate cell.

16. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a split gate cell.

20. (Twice amended herein) A method of forming a semiconductor integrated circuit, said method comprising:

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities through said gate dielectric layer and into said second region, said halogen-containing impurities having a concentration greater than 1×10^{14} carriers/cm^2, said selectively implanting at an implant energy that is about 0.1 keV to about 40 keV; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region by an oxidizing process.

21. (Twice amended herein) The method of claim 20 wherein said selectively implanting halogen-containing impurities into said first region also includes selectively implanting halogen-containing impurities into said second region such that said first region has a greater halogen concentration than said second region, said halogen concentration in said second region being greater than 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2.

22. (As filed) The method of claim 20 wherein said halogen containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

23 (As filed) The method of claim 20 further comprising forming a third thickness of dielectric material overlying a third region, said third region being spatially apart from said first region and said second region.

24. (As amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, said first region directly adjacent said second region;

forming a dielectric layer on said substrate;

masking said dielectric layer to expose said first region;

introducing a halogen-containing impurities through said dielectric layer and into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region,

said oxidizing process comprising a thermal anneal at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

25. (As previously added) The method of claim 24 wherein said introducing said halogen-containing impurities comprises an ion implantation.

26. (As previously added) The method of claim 24 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

27. (As amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired, a second region where a second oxide layer thickness is desired, and a third region where a third oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region, and a different halogen concentration in said third region than in said first region and said second region, each of said higher halogen concentration and said different halogen concentration being in excess of 1×10^{14} carriers/cm^2; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region.

28. (As previously added) The method of claim 27 wherein said performing an oxidizing process also simultaneously forms said third oxide layer thickness at said third region.

29. The method of claim 6 wherein at least one of said first and second concentrations is greater than 1×10^{14} carriers/cm^2 and less than 1×10^{15} carriers/cm^2.

30. The method of claim 20 wherein said forming said first and second thicknesses of dielectric material comprises an anneal process performed at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

31. The method of claim 30 wherein said anneal process is further performed at a pressure of about 760 Torr.